

11 MEMORY MANAGEMENT UNIT

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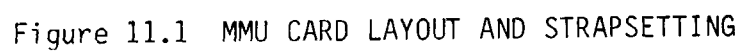
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## 11.1 MMU-IDENTIFICATIONS

Type number : PTS 6828  
Testprogram : MEMTSC (chapter14)

Power consumption : +5V 2.1A  
used only for 6813

- Straps external register address (standard /80)
- Straps interrupt level (page fault, standard /2F = 47<sub>10</sub>)

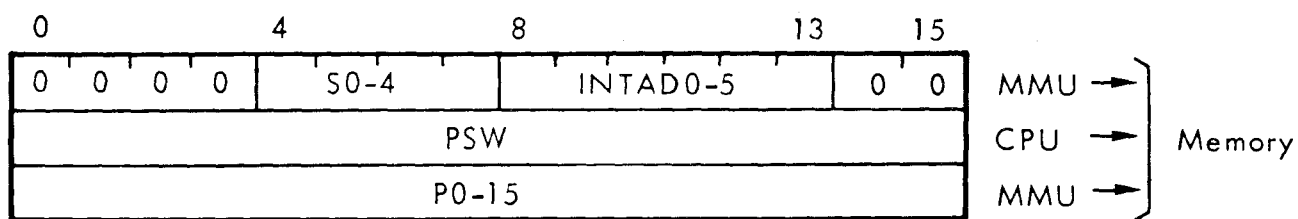


### 11.3 INTERFACE CONNECTIONS

CPU-MMU Signals		MU/CPU CONN.
BSYCPUAN	CPU has Bus control. Validates Bus signals and controls all MMU operations.	5A12
BOMFN	Table Store control signal. Page-fault stack-loading control signal: 1st -- to read aborted instruction-counter value; 2nd -- to read logic page address which set page fault and the program level of the page-fault job, coded on the MMU card.	5A21
FU = 1 = 0	CPU in User Mode. Any memory violation sets page fault CPU in System Mode.	5A22
GFETCH	Fetch cycle is executed by CPU. Instruction counter value is loaded into MMU - P-Buf register.	5A13
OSCFLO	CPU clock signal, used by MMU for internal timing.	5A17
S00-03	Logical page address from CPU P-register.	5B22, 5A23
TMMN	Table Load control signal.	5B23, 5A24
TMMU	Translation control signal; for page-address translation, memory protection check, and memory activation by the MMU.	5B24 5B25
MMU - CPU Signals		
DONEMN	MMU reply during Table Load as each segment is loaded.	5A20
MFAULTN	Page fault is detected during translation.	5B20
MMUABS	Held at 0v (inactive) when MMU card is in place.	5A19
BUS - MMU Signals		
BIOON-15N	Data used during Table Load and WER operations.	
CLEARN	Clear signa for initializing system.	
TMEN	WER instruction timing for loading the software constant into the MMU BUFTIM register.	
TRMN	Memory reply: -- During Table Load and Table Store validates data. -- During translation releases memory activation.	
MAD04-15	Address line to: -- select the MMU during instruction, and -- store the CPU instruction-counter value during each Fetch instruction cycle.	
WRITE	CPU command for store cycles. Used during translation to test for page fault (read-only page and User Mode), and sets segment table Modified-Page bit (8) of accessed page (if no page fault).	
BIOON-15N	Data used during Table Store or Page-Fault stack loading operations.	
MAD128,64 0-3	Memory address lines for physical page addresses from the segment table.	
TMRN	Activates memory during page address translation, if there is no page fault.	
TRMN	External register reply to CPU when software constant is loaded during WER instruction.	

## 11.4 HARDWARE SOFTWARE INTERFACE DETAILS

### Stack after Page Fault Interrupt



$S$  = page number

P = program counter or aborted instruction

Instructions : see P800M Programmer's Guide 1,2 and 3

Volume II Instruction set.

Loaded by TL instruction for a specific User program, and used during address translations.

SEGMENT  
TABLE  
CONTENTS

0	5	6	7	8	9	10	15
PAGE ADDRESS	PE	RO	M	O	TIMER		

Physical Page Addresses. One segment accessed for each address translation

Memory Protection:

PE -- Page Error bit is set to restrict this page to System Mode only.

RO -- Read Only bit is set to restrict this page to read operations only.

Overflow of Timer

Controlled by MMU according to number of address translations, and a "Window Interval" loaded into MMU by a WER instruction.

Modified Page is set when a write occurs on the page, indicating that the backing store is now different from the main memory.

Figure 11.2 MMU SEGMENT TABLE

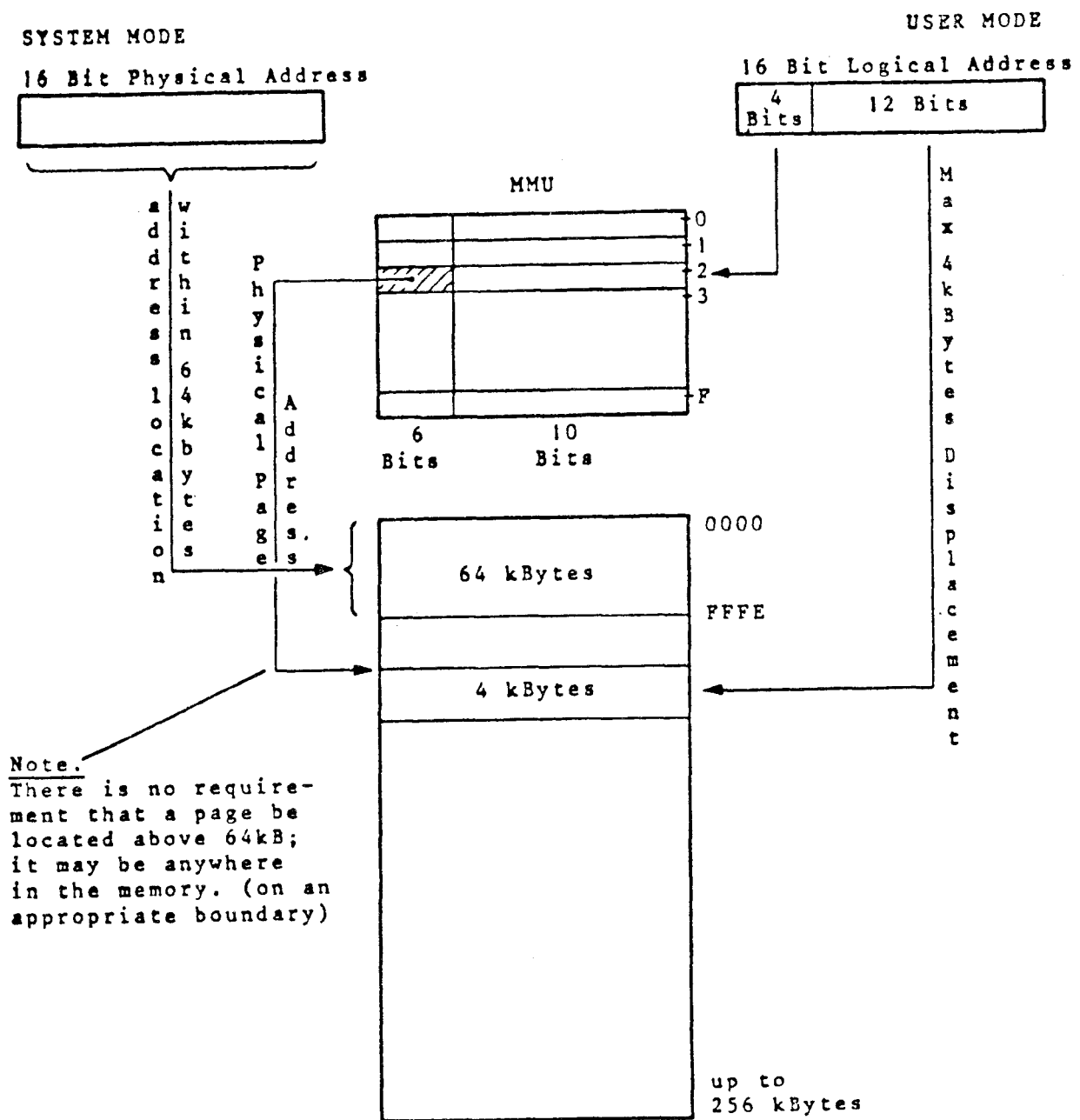


Figure 11.3 MMU MEMORY ADDRESSING

## 11.5 SHORT DESCRIPTION TESTPROGRAM

See MemTSC (rel.2) chapter 11

## 11.6 SHORT ROUTINES

DATE 04-01-80

IDENT MMUA

IDENT MMUA

\* THIS PROGRAM CHECKS THE TIMER OF THE MMU SEGMENT TABLE

\*SYSTEM PROGRAM

0100	87A0	START	AORG	/100	
0102	0400		LDKL	A15,/400	LOAD STACKPOINTER
0104	8120		LDKL	A1,/140	PROGR INTERRUPT
0106	0140				
0108	8141		ST	A1,2	
010A	0002				
010C	8120		LDKL	A1,/180	PAGE FAULT INT.
010E	0180				
0110	8141		ST	A1,/5E	
0112	005E				
0114	0100		LDK	A1,0	SET TIMING CONSTANT 0,-/FF
0116	7180		WER	A1,/80	
0118	0200		LDK	A2,0	
011A	8120		LDKL	A1,/2000	FOR SEGMENT TABLE WITH /2000
011C	2000				
011E	8149		ST	A1,/200,A2	EVERY PAGE!
0120	0200				
0122	1202		ADK	A2,2	16 MEM. WORDS/SECTOR TABLE
0124	EA20		CHK	A2,/20	
0126	0020				
0128	5A0C		RB(2)	#-10	
012A	8840		TL	/200	LOAD SEGMENT TABLE IN MMU
012C	0200				
012E	2801		SMD		GO TO USER MODE

\*USER PROGRAM

NEXT INSTR: /130 LOG =/8130 PHYSICAL

8130	0200		AORG	/8130	
8132	0355		LDK	A2,0	NO OP
8134	0400		LDK	A3,/55	
8136	8351		LDK	A4,0	
8138	3000		ST	A3,/3000,A4	/3000 LOG =/8000 PHYS.
813A	1402				
813C	EC20		ADK	A4,2	
813E	0100		CHK	A4,/100	
8140	5A0C		RB(2)	#-10	
8142	2804		LKM		CAUSES PROGRAM INTERRUPT
8144	0001		DATA	1	

\* INTERRUPT ROUTINE FOR PROGRAM INTERRUPT

0140	20FB		AORG	/140	
0142	8841		RIT	/10	RESET INTERRUPT
0144	0300		TS	/300	STORE MMU SEGMENT TABLE FROM /300 ON
0146	207F				

HLT  
\*RESTART FROM ADDRESS /100 AFTER MASTER CLEAR

\* INTERRUPT ROUTINE FOR PAGE FAULT

0180	8841		AORG	/180	
0182	0300		TS	/300	STORE SEGM TABLE MMU FROM /300 ON
0184	207F				

HLT  
\*RESTART FROM ADDRESS /100 AFTER MASTER CLEAR  
END START



# PROGRAM EXECUTION MMUA

CHECK ON TIMER: preset software counter on /100 \* Modified page

info segment table 2000, 2039, 2039, 2081, 2038 ....2038  
from add. /300

0	1	2	3	4	15
:	:	:	:	:	:
.	.	.	.	.	.

## CHECK TIME ON

OVERFLOW : change address /813E info /100 into /120

info segm. table 2000, 2040, 2040, 2081, 203F.....203F  
from add. /300

↑  
overflow!

↙ counter top-  
- count.

CHECK ON READ : change address /11C into /2000 into /2100.  
ONLY interrupt ↘ page fault (mem prot. for USER program).

CHECK ON PE : change address /11C info /2000 into /2200.  
BIT interrupt ↘ page fault (mem. prot. for SYSTEM program)  
- also for read in protected page -

/0000	int. routine address progr. int	
/0002		
/005E	int. routine address page fault	
/0100	system program	
/0140	int. routine progr. int.	
/0180	int. routine page fault	
/0200	segment table (old)	
/0300	segment table (new) (after interrupt stored)	
/03FC	page number and int. level	/03BC
/03FE	PSW	/FCC1
/0400	stack P	/0134 (e.g.)
/8000	/0055 for 80 word locations - job, used as delay -	
/8130	prog. user page 0	page 3

Figure 10.3 MEMORY USE OF MMUA